Batch wafer temperature
Oxford Instruments discuss control
Wafer temperature control in batch processing

As consolidation provides less custom for tool and materials manufacturers in the semiconductor industry, companies seek alternative markets to sell advanced tools and materials. There are opportunities for companies outside the semiconductor industry. One of these is the growing LED industry which faces its own manufacturing challenges in developing new and more powerful LEDs every year. Mark Dineen is a Principal Applications Engineer and Mike Cooke is the New Product Introduction Manager at Oxford Instruments Plasma Technology and here they discuss meeting the challenge of controlling temperature in batch wafer processing.

The throughput of a plasma etcher used for texturing sapphires depends not only on having an efficient high density plasma source, but also on the ability of the tool to remove heat from the substrates. In many plasma etch processes, there is more plasma density available, but the etch rate is limited by the survival of the photoresist mask in the face of heat fluxes of up to 1 W cm\(^{-2}\) from the high power ICP380 source.

The silicon wafer industry is accustomed to clamping single wafers to a temperature-controlled table, and introducing a heat transfer medium, normally helium gas, between the table and the wafer. ‘Helium backside cooling’ has become the standard method for single wafer temperature control. However, the HBLED manufacturing route currently uses batches of smaller substrates, passed into the etch tool on a carrier plate. This significantly affects heat transfer, by introducing a second low pressure gas interface in series with the normal wafer-table interface. Heat must now pass from wafer to carrier plate, then from carrier plate to table. The main temperature drops are at these interfaces – the temperature drops across the wafer thickness or carrier plate thickness are very small by comparison.

Results count

Figure 1 shows the temperatures of the electrode table surface (lower line) and of a single sapphire wafer (upper line) placed directly on the table, under high power etch conditions without helium backside cooling. A fibre-optic probe was used to measure temperatures in vacuum, in the presence of rf excitation.

The probe was attached to the front surface with polyimide tape, and a little Fomblin grease to measure the substrate temperature within about 5 degrees. It was also helpful to create a small ‘umbrella’ of metal foil over the sensing tip, to avoid direct heating of the tip by the plasma. Without the He cooling, the temperature of the sample placed on the electrode continues to rise over time, eventually reaching over 200\(^{\circ}\)C! An even higher temperature rise would be expected if the wafer sat on a carrier plate.
Figure 2 shows a fully loaded carrier with twelve 2” wafers in-situ. The plate is designed to deliver helium to the rear of each substrate, and to clamp the wafers in a sandwich. There is clearly space to accommodate larger batch sizes, and designs exist for up to 18 x 2” wafers.

The efficiency of the cooling is shown in Figure 3. This is the temperature of one of the batch of 2” sapphires carried on the sandwich plate. The wafer temperature is kept well below 90°C even after one hour of etching, sufficient to ensure the integrity of the photoresist.

A prime example of using this technique is Patterned Sapphire Substrate (PSS) etching for high quality GaN growth. Figure 4 shows a typical feature etched onto a wafer, this pattern is repeated across the batch of twelve wafers.

Etching large numbers of wafers with a photoresist mask requires good temperature control of each wafer, and this requires an understanding of how to transfer the heat from the plasma away from the samples to the cooled electrode. Helium backside cooling is the key, and understanding how to enable this for every wafer ensures success.

### Figure 2: 12 x 2” Sapphire Wafers ready for etching

### Figure 3: Wafer temperature during etch

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